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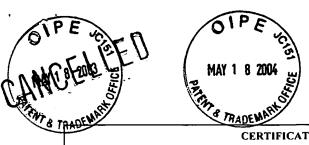
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A TRADE!	ARE		Application Number		10/066,095		
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FOR	RM		First Named Inventor		Steven Teig, et al.		
(to be used for all correspon	ndence after	initial filing)	Group Art Unit		3628		
			Examiner Name		Chencinski, S.		
Total Number of Pages in Th	is Submissi	on	Attorney Docket Number		SPLX.P0074		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/066,095

Filing Date: 1/31/2002

For: METHOD AND APPARATUS FOR

IDENTIFYING A SET OF PATHS

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to

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Dated: May 14, 2004

Respectfully submitted

Manilad

Registration No. 39,585

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Filing Date 1/31/2002 **First Named Inventor** Steven Teig et al. Group Art Unit 3628

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Examiner Name Chencinski, S.

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Application Number

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Examiner* Initials	Cite U.S. Pate Application No.1 Serial Number D			Name of Patentee or Applicant of Cited Document Name of Patentee or Applicant MM-DD-YYYY		Related Application Data if any		
	1.	10/066,060	SPLX.P0072	Steven Teig	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.		
	2.	10/066,160	SPLX.P0073	Steven Teig	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.		
	3.	10/066,047	SPLX.P0078	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.		
	4.	10/061,641	SPLX.P0079	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.		
	5.	10/066,094	SPLX.P0080	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.		
	6.	10/076,121	SPLX.P0081	Steven Teig et al.	02-12-2002	CIP of 10/066,094.		
	7.	10/062,995	SPLX.P0105	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.		
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Application Number 10/066,095 Substitute for form 1449A/PTO **Filing Date** 1/31/2002 INFORMATION DISCLOSURE **First Named Inventor** Steven Teig et al. STATEMENT BY APPLICANT Group Art Unit 3628 (use as many sheets as necessary) **Examiner Name** Chencinski, S. Attorney Docket Number 9 SPLX.P0074 of Sheet 2 U.S. PATENT APPLICATIONS 10/335,086 CDN.P0040 Steven Teig et al. 12-31-2002 13.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE (+) inside this box Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number **Application Number** 10/066,095 Substitute for form 1449A/PTO Filing Date 1/31/2002 **EORMATION DISCLOSURE First Named Inventor** Steven Teig et al. STATEMENT BY APPLICANT Group Art Unit 3628 se as many sheets as necessary) **Examiner Name** Chencinski, S. SPLX.P0074 9 Attorney Docket Number 4 NON PATENT LITERATURE DOCUMENTS Fujimura, K. et al, Homotopic Shape Deformation. Hama, T. et al., Curvilinear Detailed Routing Algorithm and its Extension to Wire-Spreading and Wire-29. Fattening. Hama, T. et al., Topological Routing Path Search Algorithm with Incremental Routability Test, IEEE 30. Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, No. 2, February 1999, pp. 142-150. Kobayashi, K. et al., A New Interactive Analog Layout Methodology based on Rubber-Band Routing, UCSC-CRL-96-12, June 13, 1996. Lim, A. et al, A Fast Algorithm To Test Planar Topological Routability, Technical Report 94-012, pp. 1-32. 16. Lu, Y., Dynamic Constrained Delaunay Triangulation and Application to Multichip Module Layout, A 33. Thesis for Master of Science, UC Santa Cruz, December 1991. Maley, F.M., Testing Homotopic Routability Under Polygonal Wiring Rules, Algorithmica 1996, 15: 1-16. 34. Morton, P. B. et al., An Efficient Sequential Quadratic Programming Formulation of Optimal Wire Spacing for Cross-Talk Noise Avoidance Routing, UCSC-CRL-99-05, March 10, 1999. NN71091316, Use of Relatively Diagonal And Rectangular Wiring Planes n Multilayer Packages, 36. September 1971, IBM Technical Disclosure Bulletin, Vol. No. 14, Issue No. 4, pp. 1316-1317. Staepelaere, D. et al., Geometric Transformations for a Rubber-Band Sketch, A Thesis for a Master of 37. Science in Computer Engineering, UCSC, September 1992. Staepelaere, D. et al., Surf: A Rubber-Band Routing System for Multichip Modules, pp 18-26, 1993. 38. Su, J. et al., Post-Route Optimization for Improved Yield Using Rubber-Band Wiring Model, 1997 39. International Conference on Computer-Aided Design, pp 700-706, November 1997. Wei-Ming Dai, W. et al., Routability of a Rubber-Band Sketch. 28th ACM-IEEE Design Automation 40. Conference, 1991. pp. 45-65.

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Based on PTO/SB/08 a & b (05-03) Approved for use through 05/31/2003. OMB 0651-0031 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE +) inside this box 1 Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number **Application Number** 10/066,095 Substitute for form 1449A/PTO Filing Date 1/31/2002 INFORMATION DISCLOSURE **First Named Inventor** Steven Teig et al. ATEMENT BY APPLICANT Group Art Unit 3628 8 2004 (use as many sheets as necessary) **Examiner Name** Chencinski, S. TRADENT SPLX.P0074 9 9 Attorney Docket Number Shee 10 NON PATENT LITERATURE DOCUMENTS Schiele, W. et al., A Gridless Router for Industrial Design Rule, 27th ACM-IEEE Design Automation Conference, pp. 626-631, 1990. Sekiyama, Y. et al., Timing-Oriented Routers for PCB Layout Design of High-Performance Computers, 104. International Conference on Computer Aided Design, pp 332-335, November 1991. Soukup, J. et al., Maze Router Without a Grid Map, IEEE, 1992, pp. 382-385. Takashima, Y. et al, Routability of FPGAs with Extremal Switch-Block Structures, IEICE Trans. Fundamentals, vol. E81-A, No. 5, May 1998, pp. 850-856. Teig, S. The X Architecture: Not your Father's Diagonal Wiring, International Workshop on System Level Interconnect Prediction, pp. 33-37, April 2002. Thakur, S. et al., Algorithms for a Switch Module Routing Problem, 1994, pp. 265-270. 108. 109. Theune, D. et al., HERO: Hierarchical EMC-constrained routing, 11/1992, IEEE pp 468-472. Tollis, I. Techniques for Wiring in Non-Square Grids, pp. 66-69, May 1989. Urrutia, J., On the Number of Internal and External Visibility Edges of Polygons, Department of CS, University of Ottawa, ON, Canada, February 11, 1997. Wang, D., Novel Routing Schemes for IC Layout, Part I: Two-Layer Channel Routing, 28th ACM/IEEE Automation Conference, 1991, pp.49-53. Yan et al., Three-Layer Bubble-Sorting -Based Non-Manhattan Channel Routing, ACM Transactions on Design Automation of Electronic Systems, Vol. 5, No. 3, July 2000, pp.726-734. Zhou, H. et al., An Optimal Algorithm for River Routing with Crosstalk Constraints, 1996 Zhou, H. et al., Optimal River Routing with Crosstalk Constraints, ACM Transactions on Design Automation of Electronic Systems, vol. 3, No. 3, July 1998, pp. 496-514.

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